Design and Simulation of Soft Switched Interleaved Boost Converter in Continuous Conduction Mode for RES

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Abstract— In this paper, an interleaved soft switching boost converter employing ZVS and ZCS principle leads to reduce ripple contents and high efficiency is proposed for renewable energy systems (RES).The conventional hard-switched interleaved converter results in increased switching losses and ripples. To overcome, this drawback, a two-phase Interleaved Boost Converter (IBC) with ZVS and ZCS is proposed. This circuit consists of two identical boost converter connected in parallel and are controlled by interleaved switching signals.The circuit is analyzed in Continuous Conduction Mode (CCM) with various load ranges having duty cycle of more than 50%.Simulation studies of the proposed converter is carried out in MATLAB. The performance parameters such as output voltage ripple, output current ripple, inductor current ripple and efficiency of the proposed converter is computed to show the significance of the soft switching principle.The results are verified.

Index Terms— Interleaved Boost Converter (IBC); soft switching; Zero Voltage Switching (ZVS); Zero Current Switching(ZCS); Continuous Conduction Mode (CCM)

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1 INTRODUCTION

Power electronics will play a vital role in energy saving. Energy efficiency can make a major contribution to meeting the global energy demand. A boost converter is a particular type of power converter with an output DC voltage greater than the input. This type of circuit is used to 'step-up' a source voltage to a higher, regulated voltage, allowing one power supply to provide different driving voltages.In recent years, interleaved boost converter is well suited for high performance applications. The advantages of IBC include increased efficiency, reduced size, reduced electromagnetic emission, faster transient response and improved reliability.

The switching losses pre-dominate causing junction temperature to rise which is a major drawback of PWM switching. The soft switching phenomena known as zero-voltage switching (ZVS) and zero-current switching (ZCS) can reduce switching losses. For zero-voltage switching (ZVS), the transistor will be turned on at zero Vds voltage to reduce the turn on switching loss. For zero-current switching (ZCS), the transistor will be turned off at zero Id current to reduce the turn off switching loss. The soft switching techniques reduce the switching losses enabling high frequency operation and consequently reducing the overall system size and hence to increase the power density.

The passive snubber circuits can be added to the converter to reduce the stresses to safe levels by limiting the rate of rise (di/dt) of currents through devices at device turn on and limiting the rate of rise (dv/dt) of voltages across devices during reapplied forward blocking voltages and shaping of the switching trajectory of the device as it turn on and off.

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2 CIRCUIT CONFIGURATION

2.1 Cicuit Construction

Fig. 1 shows the proposed soft switching interleaved boost converter module. DC-DC boost converters are connected in parallel which leads to reduction of the size of components especially inductors. The total power is divided in paralleled converters there by reduceing the stress among the individual converters. In this paper, an $N = 2$ parallel boost converter structure with one output capacitor is considered as shown in fig.1.

The interleaving technique ensures the reduction of ripple currents in both input and output circuits. In the circuit construction, the output current is split into two paths, substantially reducing I^2R losses and inductor AC losses. There by higher efficiency is realized.

The MOSFETs with appreciable on-state current-carrying capability and off-state blocking voltage capability are potential candidate for power electronic applications.The diodes are placed in anti-parallel with the switches. A large value of capacitor is placed at the output to ensure the desired output voltage with negligible harmonics available at switching frequency.Fig. 2 show the equivalent circuit of the converter in which the coupled inductor can be illustrated with three uncoupled inductors.

2.2 Figures

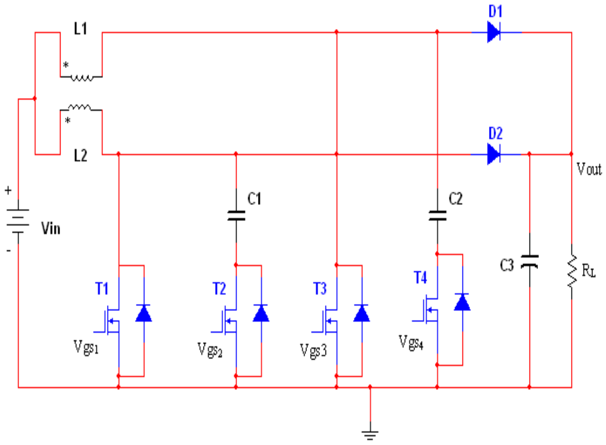

Fig. 1. Interleaved ZVS-ZCS boost converter.

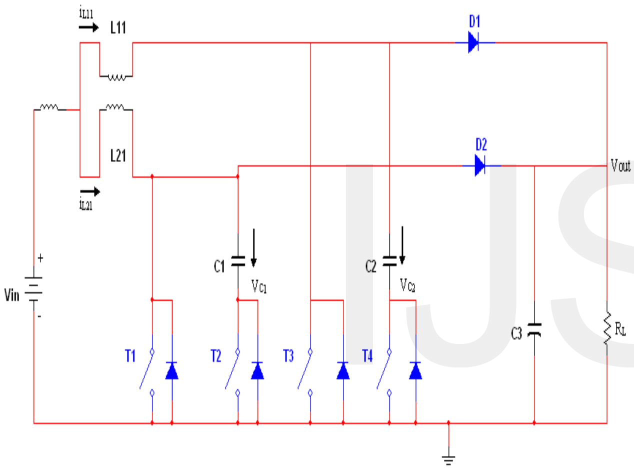

Fig. 2. Equivalent Circuit of the Converter.

3 DESIGN GUIDELINES

In the proposed soft switched IBC, the inductors at front end in an IBC are magnetically coupled to improve the electrical performance. 1. The four switches in Fig. 1 can be divided as two main switches T1 and T3 and two auxiliary switches T2 and T4.2. The coupled inductor in the boosting stage helps higher current sharing between the switches.3. The overall ripple and total harmonic distortions are reduced in this technique without sacrificing the performance and efficiency of the converter.

The interleaved boost converter design involves selection of duty cycle, boost inductances L1 and L2, the values of coupling coefficient k, the values of snubber capacitances C1 and C2. The calculations are done by the use of following equations. The duty cycle is calculated as

$$\text{Duty Cycle D} = \frac{1}{2}\left(1 - \frac{\text{Vin}}{\text{Vout}}\right) \qquad (1)$$

Vin = Input voltage
Vout = Desired output voltage
η = Efficiency of the converter, estimated 99%

Inductor Ripple Current Estimation:

$$\Delta I_L = (0.2 \text{ to } 0.4) \times I_0 \times \left(\frac{V_{out}}{V_{in}}\right) \qquad (2)$$

ΔI_L = Estimated inductor ripple current
I_0 = Necessary output current
V_{out} = Desired output voltage
V_{in} = Input voltage

Calculation of Boost Inductor Values:

$$\text{Inductances L1 and L2 are } = \frac{V_{in} \times (V_{out} - V_{in})}{\Delta I_L \times f_s \times V_{out}} \qquad (3)$$

V_{in} = Input voltage
V_{out} = Desired output voltage
ΔI_L = Estimated inductor ripple current
f_s = Switching frequency of the converter

Average Forward Current of Rectifier Diode:

$$I_f = I_0 \qquad (4)$$

I_0 = Necessary output current

Power Dissipation in Rectifier Diode:

$$P_d = I_f \times V_f \qquad (5)$$

I_f = Average forward current of the rectifier diode
V_f = Forward voltage of the rectifier diode

Output Voltage Ripple:

$$\Delta V_{out} = ESR \times \left(\frac{I_0}{1-D} + \frac{\Delta I_L}{2}\right) \qquad (6)$$

ESR = Equivalent series resistance of the used output capacitor
I_0 = Necessary output current
D = Duty cycle
ΔI_L = Inductor ripple current

Output Capacitance:

$$C_0 = \frac{I_0 \times D}{f_S \times \Delta V_{out}} \qquad (7)$$

I_0 = Necessary output current
D = Duty cycle

f_s = Switching frequency of the converter
ΔV_{out} = Desired output voltage ripple

The conduction losses of the main switches and reverse recovery losses of the diodes are greatly reduced by choosing the value of K = 0.98.The main switches are turn-off, during that period the snubber capacitors C1 and C2 tends to reduce the turn-off loss. The large value of capacitors drastically reduces the loss. But, in turn increase the energy storage capacity, will increase peak value of the current and conduction losses of the switches. So, tradeoff takes place when the value of snubber capacitors is calculated.

4 SIMULATION RESULTS

4.1 Figures and Tables

System modeling is possibly the most important phase in any form of system control design work. The choice of a circuit model depends on objectives of the simulation. Designing converters involves simulations using Matlab's Simulink program. The Table1 shows simulation parameters for the proposed circuit .In designing DC-DC converters, control of average output voltage (Vout) can be achieved by controlling the switch on and off durations (Ton and Toff). One way of controlling output voltage is by switching at a constant frequency and adjusting the on-duration of the switch in order to control average output voltage.

TABLE I.
SIMULATION PARAMETERS

COMPONENT	PARAMETER
VIN(INPUT VOLTAGE)	100 V
SWITCHING FREQUENCY	4 KHZ
DUTY CYCLE	0.39
VOUT (OUTPUT VOLTAGE)	450.5 V
OUTPUT CURRENT	0.62-3.2 A
OUTPUT POWER	300-1000 W
BOOST INDUCTORS L1 AND L2	0.6 MH
SNUBBER CAPACITORS C1 AND C2	1470 µF
OUTPUT FILTER C0	1920 µF
MOSFET ON-STATE RESISTANCE RON	0.1 Ω
DIODE ON-STATE RESISTANCE RD	0.01 Ω

Figure 3 represents controlled gating signals applied to all the four MOSFET switches. For this specific design, a switching frequency of 4 kHz is selected in order to achieve the desired output and the inductor and capacitor are determined based on this value. The inductor and capacitor are lossless. The response of the circuit is periodic. The value of inductor current at the start and end of a switching cycle is the same. The net increase in inductor current over a cycle is zero. The inductor current is continuous and greater than zero. When the switches are ON and OFF, changes in capacitor voltage can be neglected for calculating change in inductor current and average output voltage. Results for this specific design were obtained using the Simulink and are presented in Figure. 4. As shown, simulated results are in close agreement with expected theoretical results. Expected steady state output voltage at the output terminal of the circuit was 450.5 V.

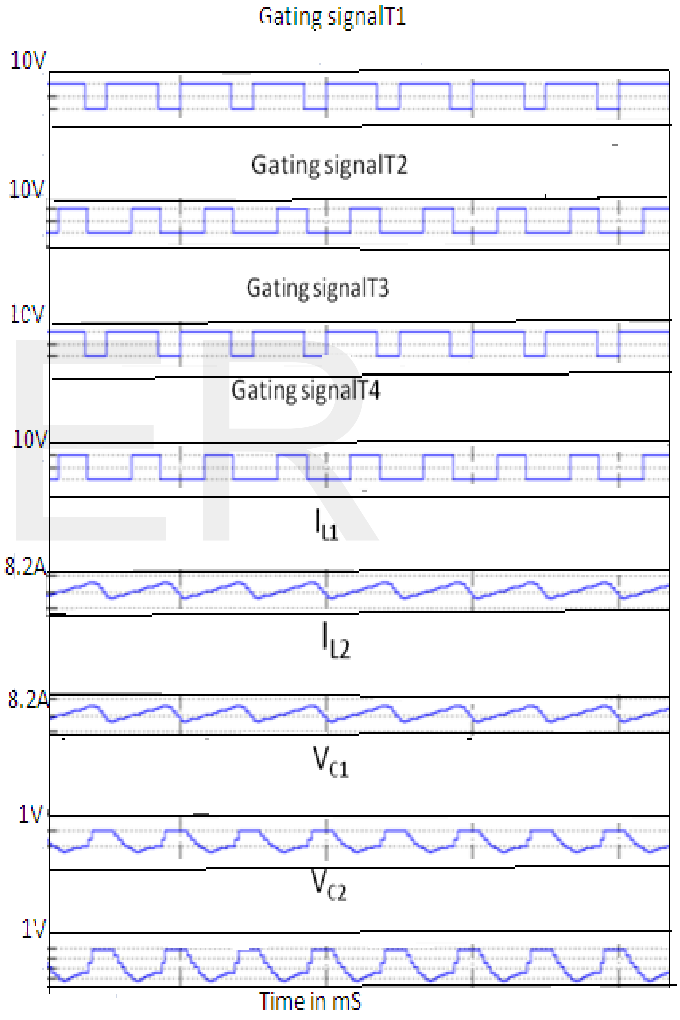

Fig. 3. Simulated Waveforms of gating signals, resonant inductor and resonant capacitor waveforms

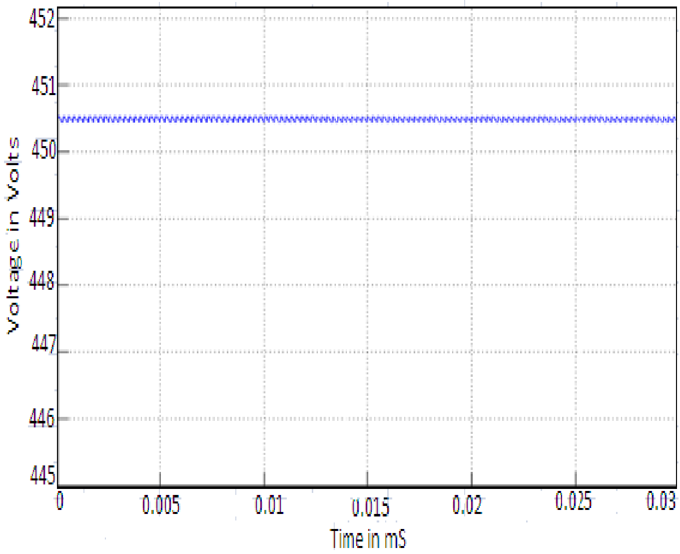

Fig. 4. Output Voltage Waveform under steady -state condition.

For this particular design, a single resistance is connected in parallel to the capacitor. The load consists of different values of resistances of low value were initially connected to calculate the output voltage ripple as shown in Figure 5.

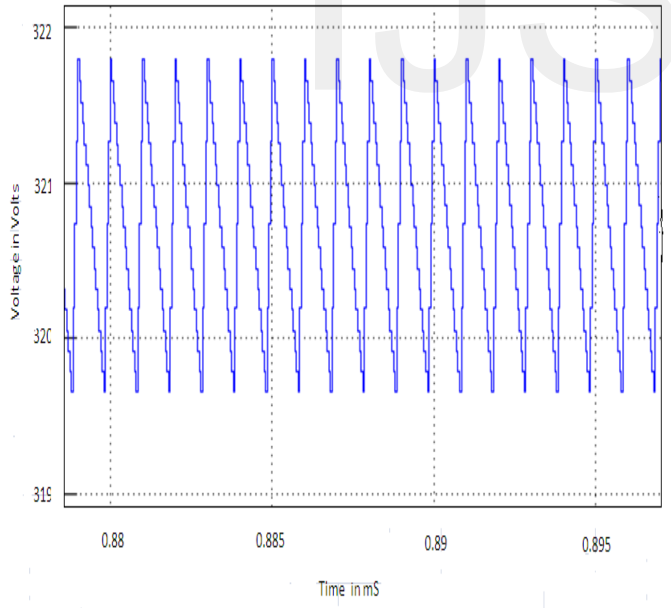

Fig. 5. Output Voltage Ripple Waveform
Output Voltage Ripple is =0.62 %

The output current ripple, input inductor current ripple and Inductor Branch Current Ripple waveforms of IBC have been shown in Figures. 6, 7 and Fig. 8.

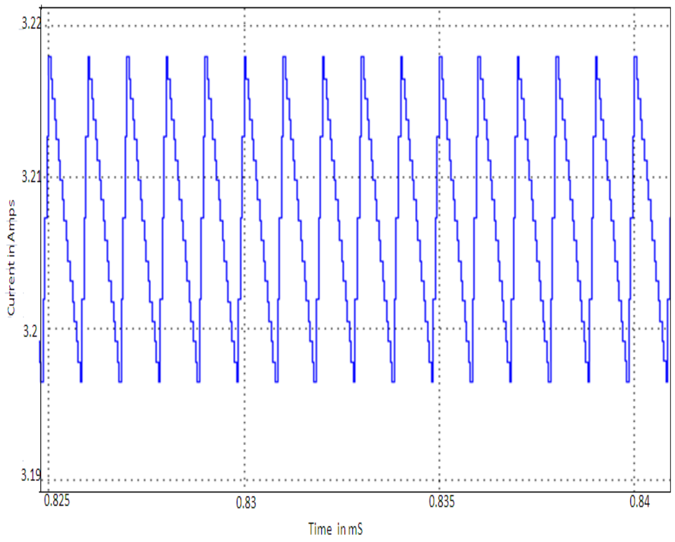

Fig. 6. Output Current Ripple Waveform
Output Current Ripple is = 0.62 %

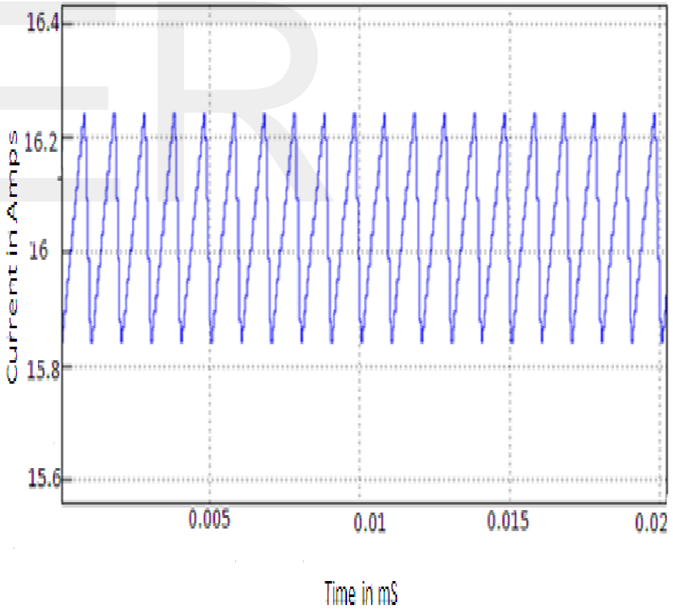

Fig. 7. Input Inductor Current Waveform
% Input Inductor Current Ripple is = 2.47 %

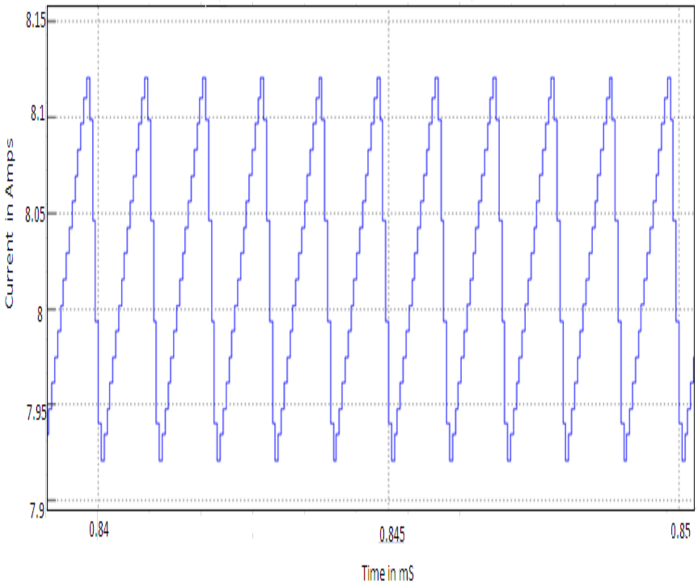

Fig. 8. Input Inductor Branch Current Waveform
% Inductor Branch Current Ripple is =2.34 %

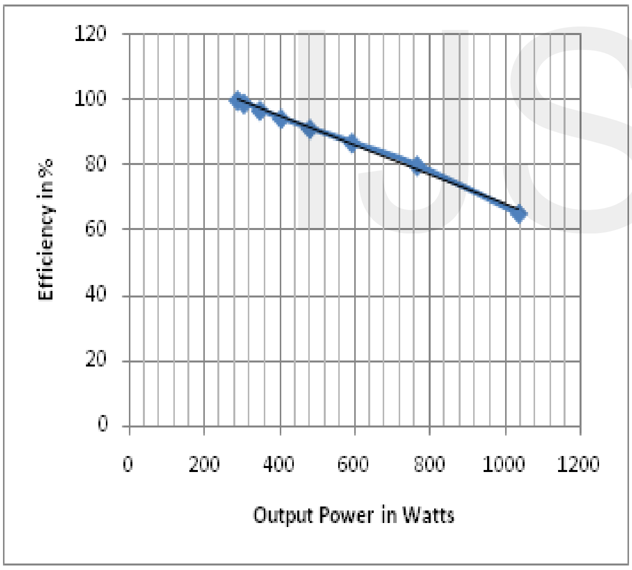

Fig. 9. Efficiency Measurement for Soft Switching Interleaved Boost Converter

The converter can withstand wide changes in load variations and the graph for efficiency versus out power is graphically shown in Fig. 9.

5 CONCLUSION

A soft switching interleaved boost converter with both zero-voltage switching and zero-current-switching techniques is dealt clearly in this paper. The equations have been presented to calculate power stage components. The duty cycle of this converter was designed to more than 50%. The various waveforms of gating signals, resonant inductor and resonant capacitor waveforms, output voltage under steady state condition, output voltage ripple, output current ripple, input inductor current ripple and input inductor branch current ripples of IBC have been simulated using MATLAB SIMULINK and expressed in terms of percentage values. The IBC having the greater advantages of higher efficiency and reduced ripple contents can be well understood from the simulation results. The output power versus efficiency has been discussed for various ranges of load.Hence, soft switched IBC proves to be a suitable topology for renewable energy sources.

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